

Introduction to 'Supreme-K' project and Beyond

* Supreme-K : National Supercomputer Development Project

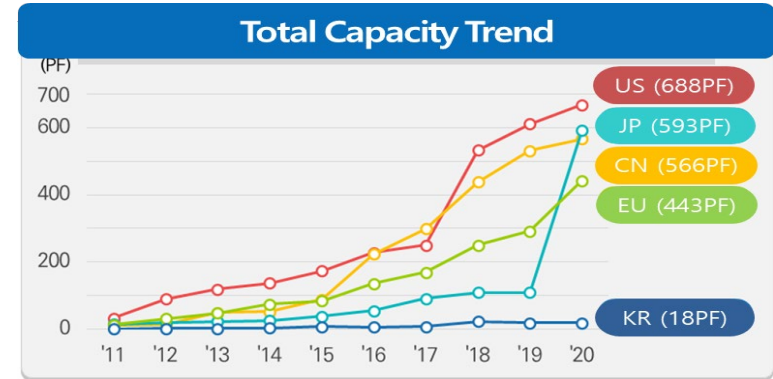
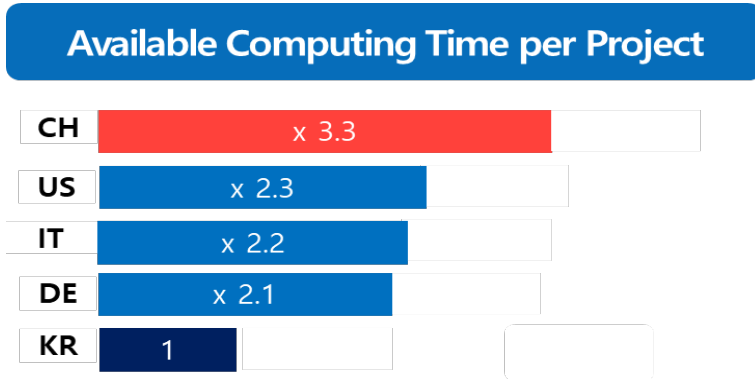
2024. 8. 21

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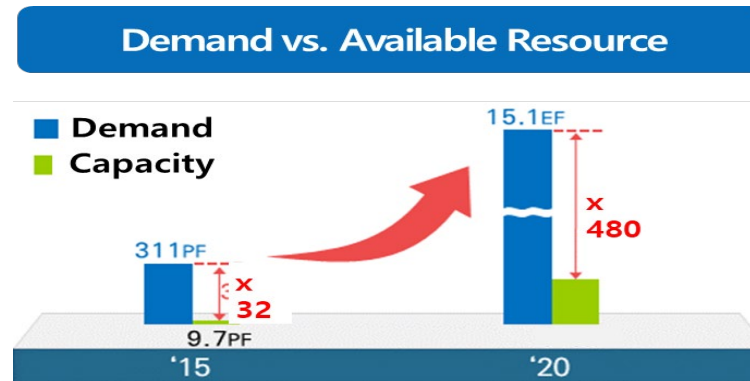
ETRI

Background – Why

❖ Not enough HPC resources in Korea (investigated in 2020)



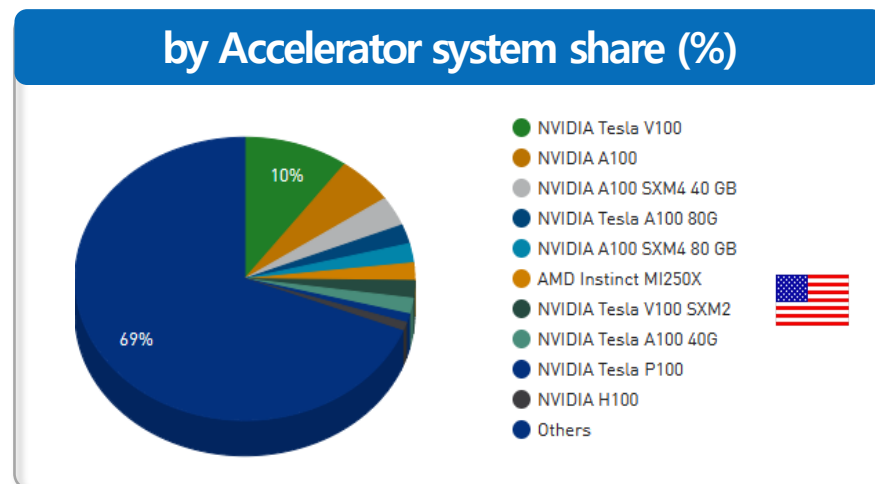
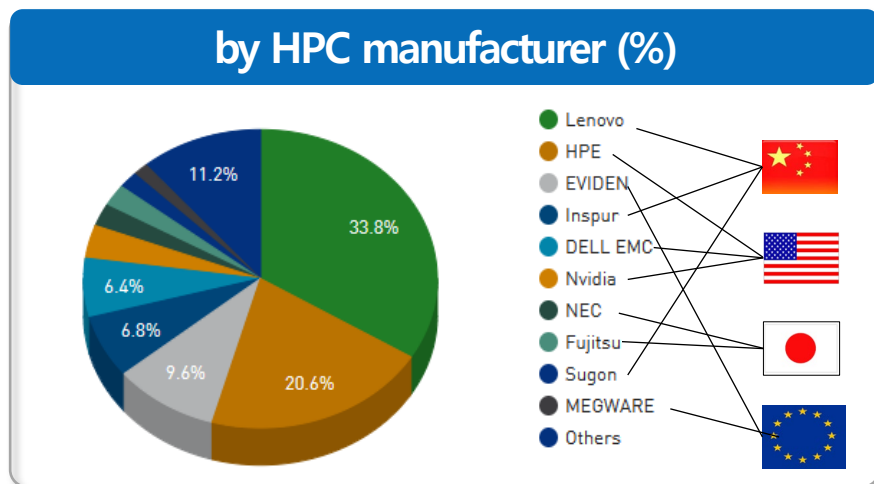
❖ HPC demand (science, industry,...) >> Available HPC resources



❖ HPC demands are increasing more and more!

Background - What

- ❖ Purchase a leading supercomputer from global vendors!
- ❖ Leading and dominant HPC and Accelerator vendors! How can we compete with them?



Background - How

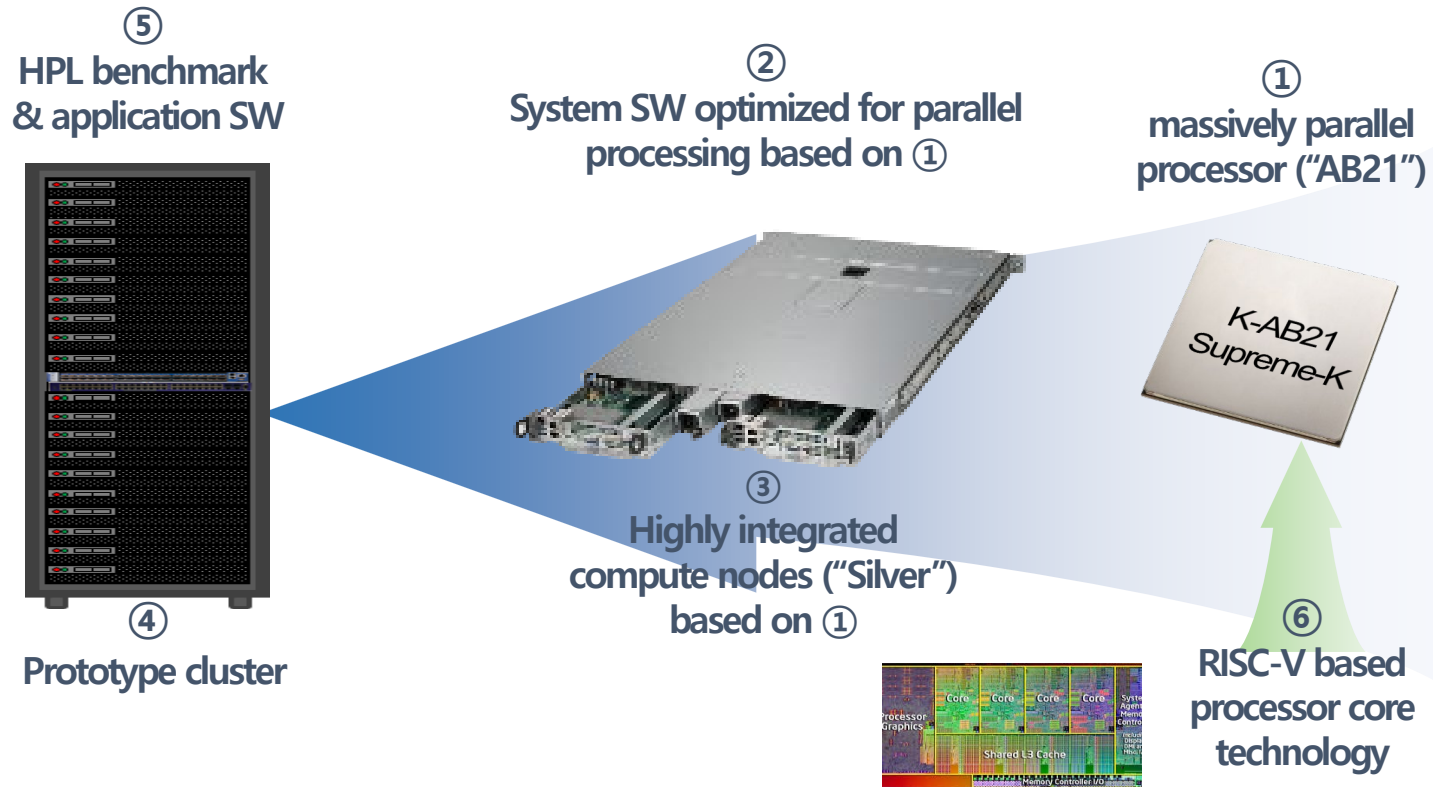
- ❖ Execution Strategy : 3-Pillars of undertaking
- ❖ Being realized through R&D projects by government



**Nation-wide Collaboration
to build Sustainable Top-tier HPC ecosystem**

Project 'Supreme-K'

- ❖ Goal: Development of a PoC of HPC system based on an in-house developed HPC accelerator('AB21'), system SWs, and compute nodes supported by Ministry of Science & ICT of Korea
- ❖ Period : Jul. 2020~Dec. 2024, Budget : ₩46.9B
- ❖ Project leader : Dr. Woojong Han, ETRI



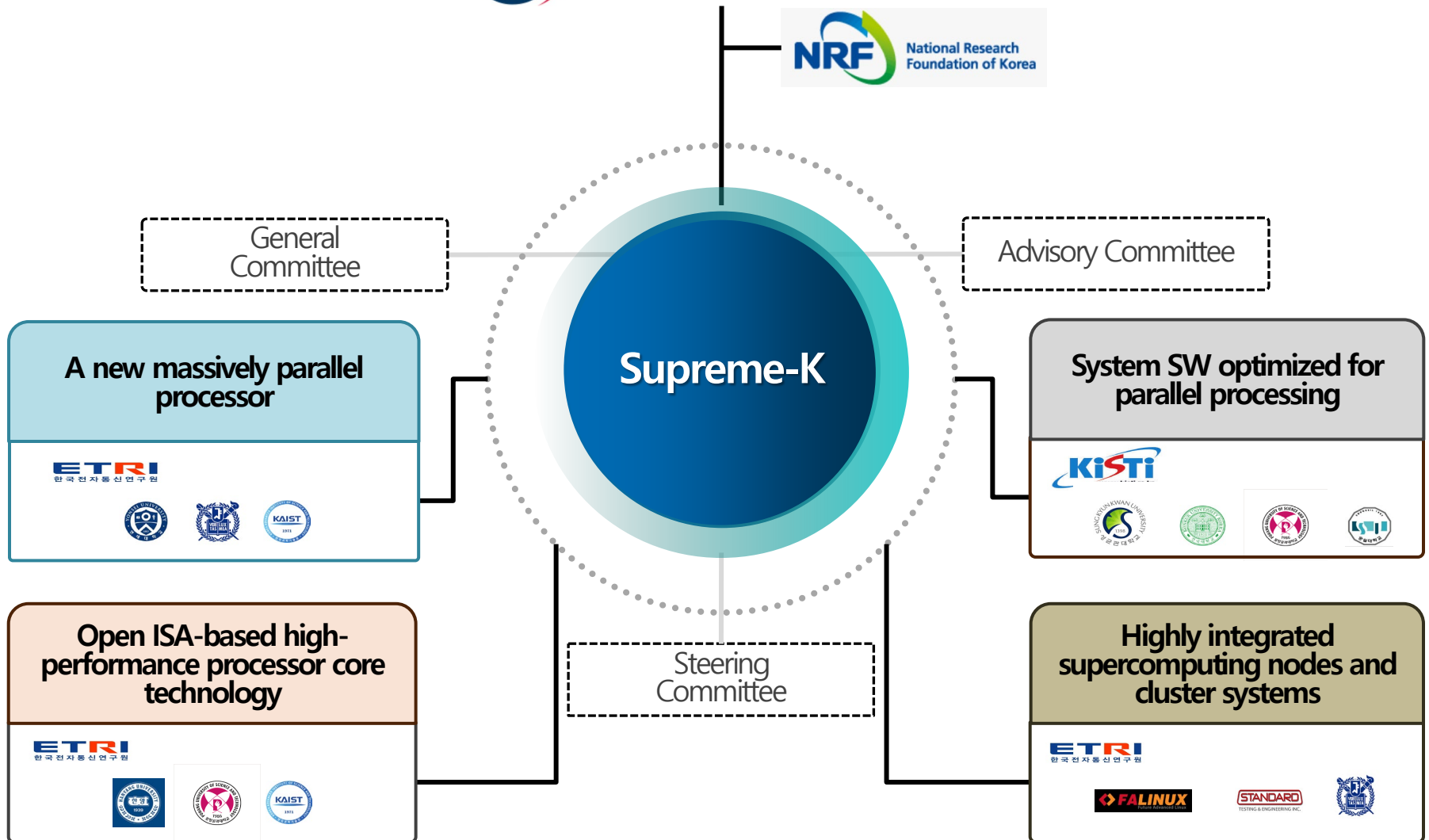
National Grand Consortium



Ministry of Science and ICT

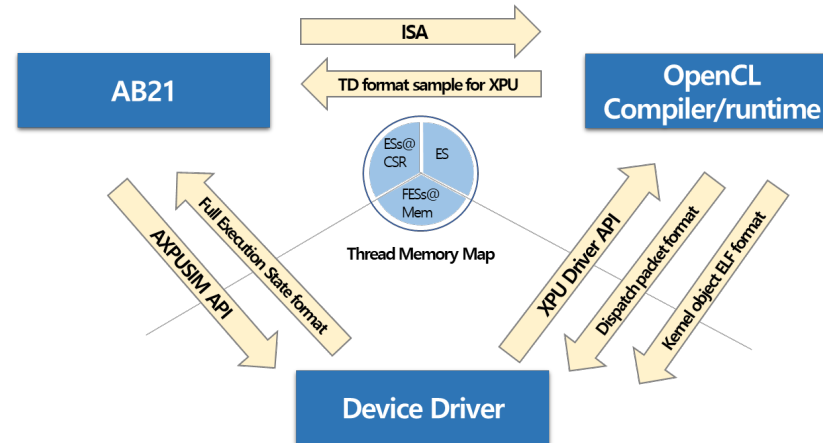


National Research
Foundation of Korea



R&D Strategy

- ❖ HW/SW Co-design for AB21(Extremely Parallel Processing Unit for FP64/FP32)



- ❖ Optimization of Data movement
 - Data sharing in shared virtual memory between Host and AB21
- ❖ Systematic Verification for System integration
 - SW simulation, FPGA-based HW emulator, SVP(Silicon Virtual Prototyping)
- ❖ Project Management
 - System/Document Configuration management
 - Issue/Risk management
- ❖ Prior research on expanding memory capacity to tackle the memory wall issue
 - another presentation

HPC accelerator("AB21) + Compute Node("Silver)

~4Q, 2023

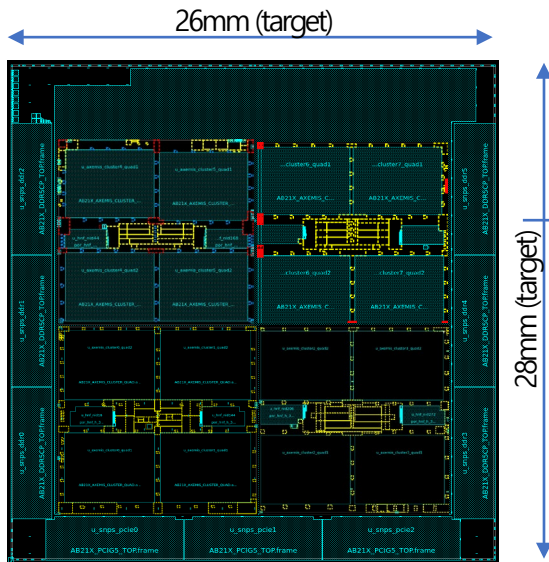
SW Requirement from HPL,
Design & validation of AB21,
Floor planning

~2Q, 2024

① AB21 chip
- Rpeak: 8TFLOPS@FP64

~4Q, 2024

③ Compute Node for AB21
- Rpeak: 16TFLOPS@FP64

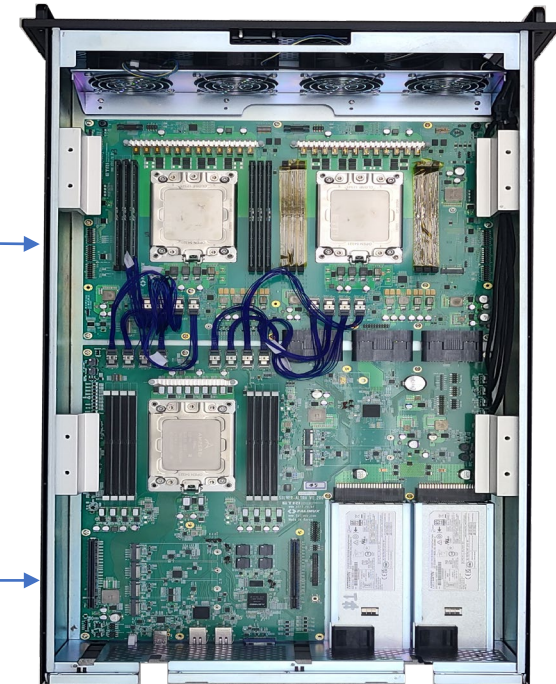


AB21 Floor plan after BE



(@TSMC, 12nm)

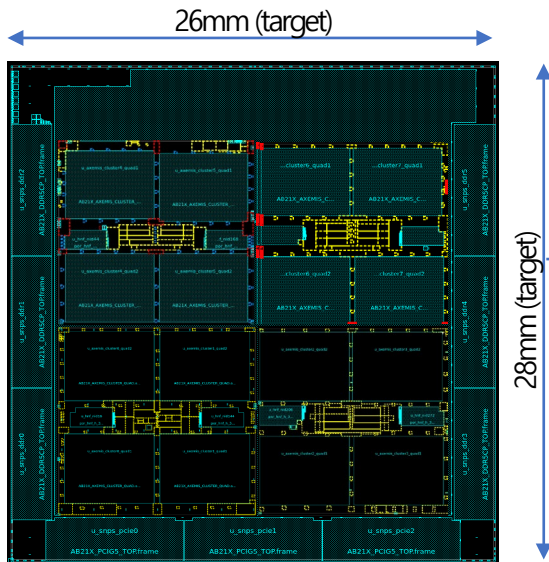
② SW stacks for AB21



HPC accelerator("AB21) + Compute Node("Silver)

~4Q, 2023

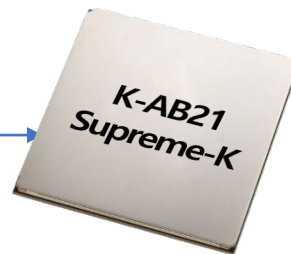
AB21 Floor plan



~2Q, 2024

① AB21 chip

- Rpeak: 8TFLOPS@FP64



(@TSMC, 12nm)

~4Q, 2024

③ Compute Node for AB21

- Rpeak: 16TFLOPS@FP64

- XEC : eXecution Core
- XEM : XcElerator for Matrix-multiplication
- XECM : XEC + XEM
- XEMIS : XcElerator for Matrix-multiplication and Input data Sharing
- XPU : parallel eXecution Processing Unit

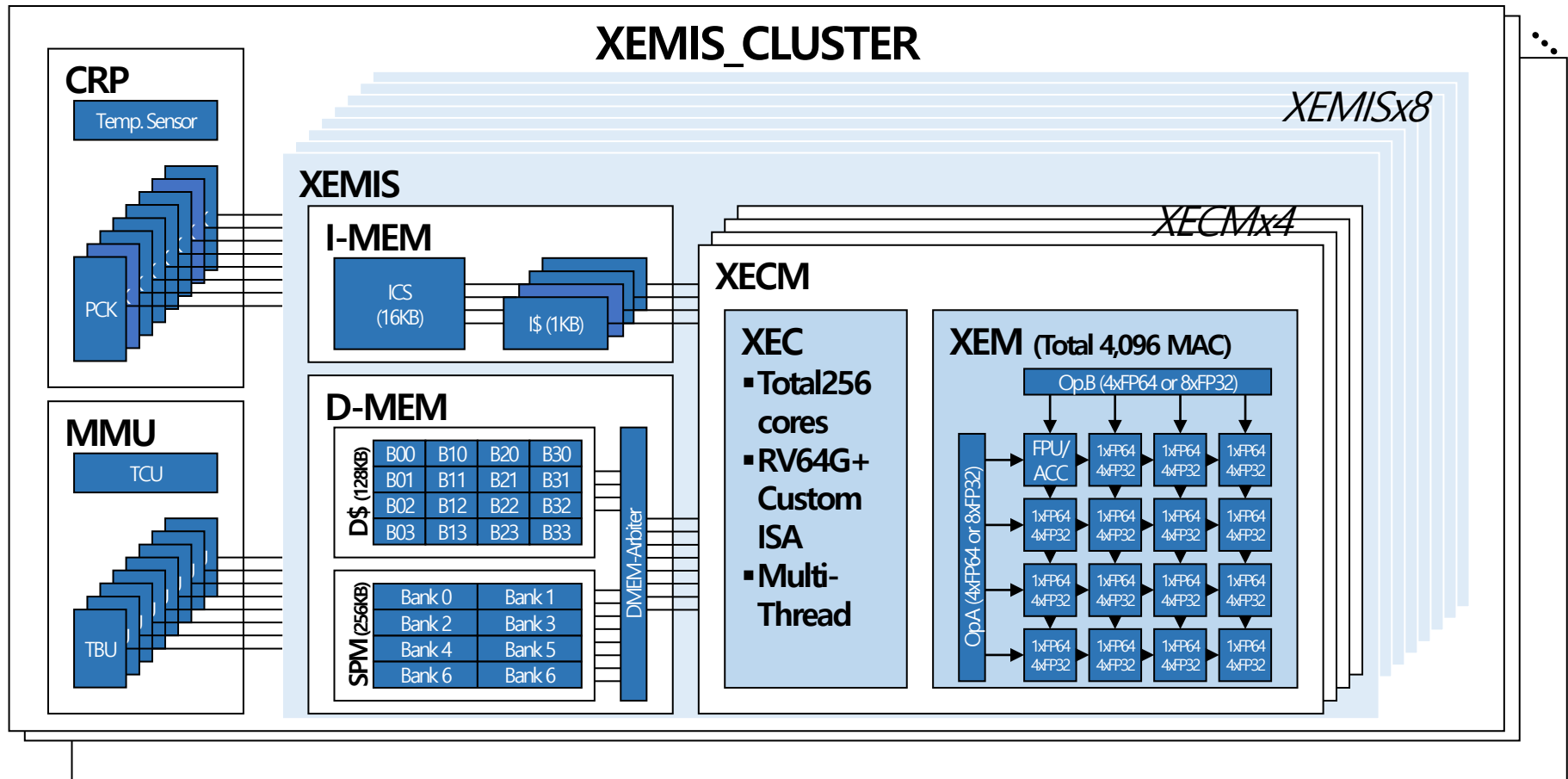
Rpeak	▪ 8TFLOPS@FP64 ▪ 32TFLOPS@FP32
NoC	▪ ARM CMIN-700
PE	▪ ARM Neoverse-V1 * 2
Parallel Processing Unit (next page)	▪ XEMIS cluster * 8 ▪ XEMIS * 8 ▪ XECM * 4 - XEC(256 cores) : RV64G+Custom ISA - XEM(FP64 4096 cores) : FP64, FP32 Multi-precision Matrix Multiplication
Memory	▪ DDR5 6 ch.* 64GB = 384GB
PCIe	▪ PCIe Gen5 16 lane * 3ch.
Cache/SPM	▪ D-Cache(128KB*16) + SPM(256KB*16)
Gates	▪ 1.4 billion gates ▪ approximately 4,900 balls
Die size	▪ 26mm x 28mm

* Chun-gi Lyuh et. al, "Development of SoC to Accelerate 64/32 bit floating point matrix calculation for Supercomputers," JCCI 24, Apr. 2024.

HPC accelerator("AB21) + Compute Node("Silver)

❖ Parallel Processing Unit in AB21

XEMIS_CLUSTER x 8



HPC accelerator("AB21) + Compute Node("Silver)

~4Q, 2023

AB21 Floor plan

~2Q, 2024

① AB21 chip
- Rpeak:8TFLOPS@FP64

~4Q, 2024

③ Compute Node for AB21
- Rpeak: 16TFLOPS@FP64

② SW stacks for AB21



OpenCL Compiler
(LLVM/Clang 16)

Analysis & Dev tools

Auto tuning

OpenCL Debugger
(LLVM/LLDB 16)

Profiler
(PAPI)

HPC Benchmark

HPL v2.3
(Netlib HPL)

QAND
(In-house simulation code)

Math library

BLAS for AB21
(CLBlast 1.5.1)

ARMpl 20.3.0

Programming model

OpenCL Runtime
(SoCL v1.0)

MPI
(MVAPICH2 2.3.7)

Low-level I/F library

XDL v3.0

Management

xpu-smi

Operating system (Ubuntu 22.04 LTS)

AB21 Device Driver

HPC accelerator("AB21) + Compute Node("Silver)

~4Q, 2023

AB21 Floor plan

~2Q, 2024

① AB21 chip
- Rpeak:8TFLOPS@FP64

~4Q, 2024

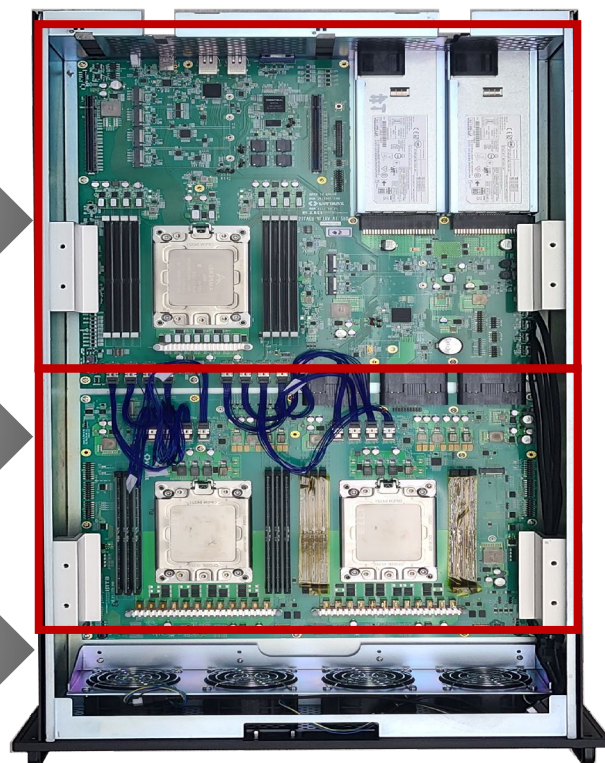
③ Compute Node for AB21
- Rpeak: 16TFLOPS@FP64

Host board	- ARM CPU (Ampere) - BMC FW (OpenBMC) - BIOS FW (UEFI) - DDR4 64GB * 8 ch. - PCIe Gen4 * 2ch.
AB21 board (i.e. Accelerator board)	- AB21 x 2 - DDR5 x 6 ch. - PCIe G5 x 3 ch.
Enclosure	19" standard chassis/3U - Hybrid(Air + Liquid) cooling

Host board

AB21 board

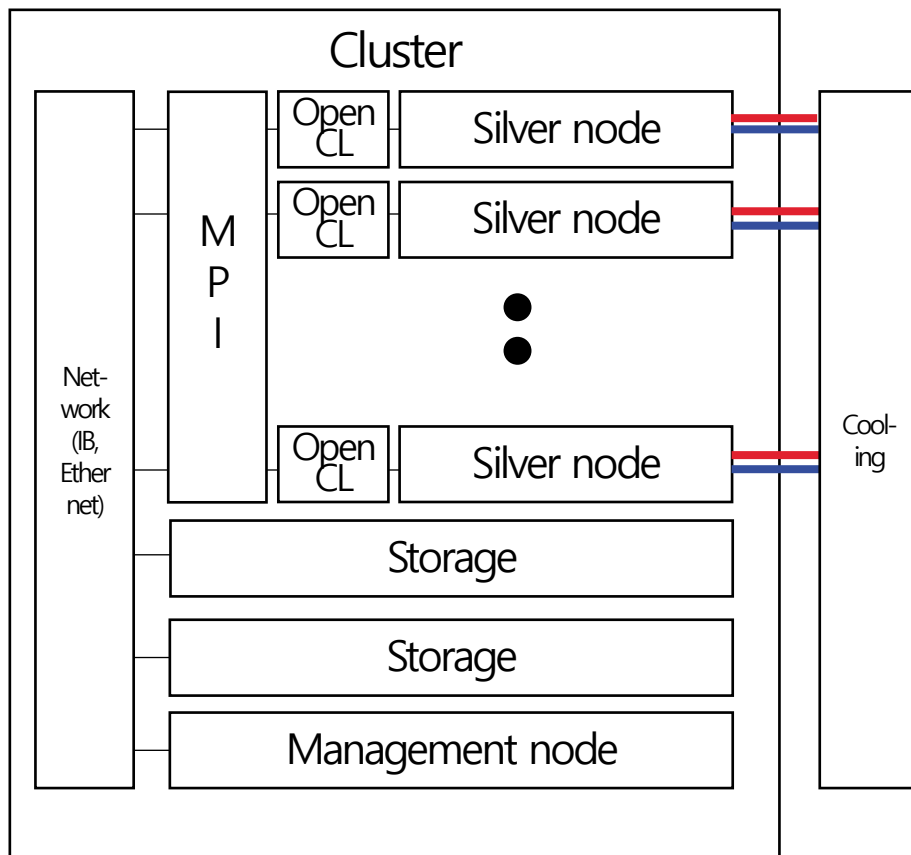
Enclosure



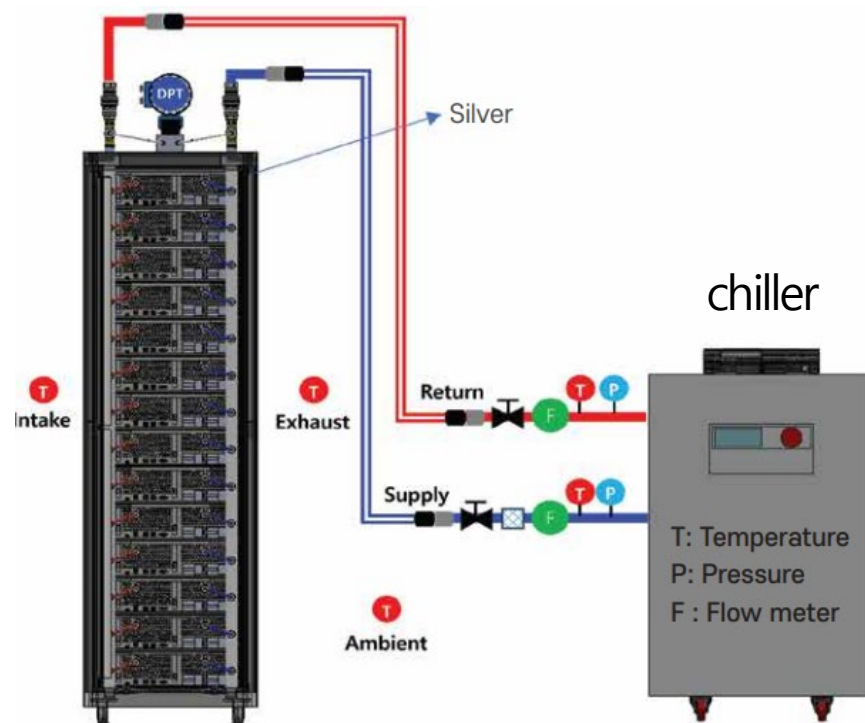
Single-rack scale Cluster Systems

= 8 Silver nodes+1 Management node+2 Storage nodes+IB/Ethernet+Liquid cooling

❖ Logical view



❖ Physical view



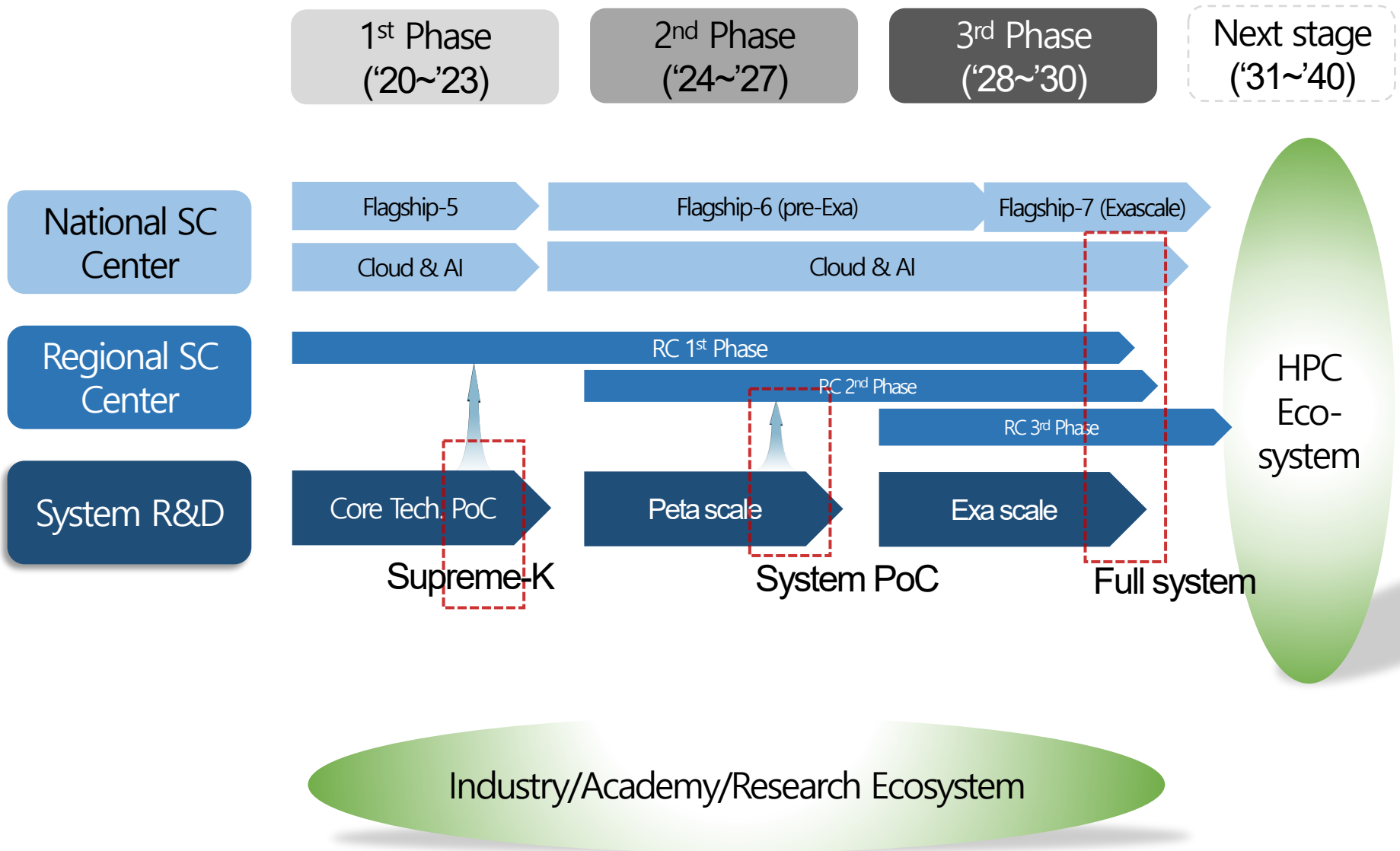
Single rack-scale cluster
with Partial 2PC(2 Phase liquid Cooling)*

* Woo-Jung Shin et al, "Development trend of cooling system for HPC with refrigerant contact method focusing on the highest cooling performance," JCCI 24, Apr. 2024.



Beyond 'Supreme-K' in Korea

HPC roadmap in Korea('21.5)



Looking into the future

Supreme-K

A stepping stone for the full scale HPC system in Korea ('20~'24)

HPC
Accelerator

System SW
optimized
for Supercom
CPU

Highly
Integrated
computing
nodes

RISC-V based
processor
core

Platform core
technology

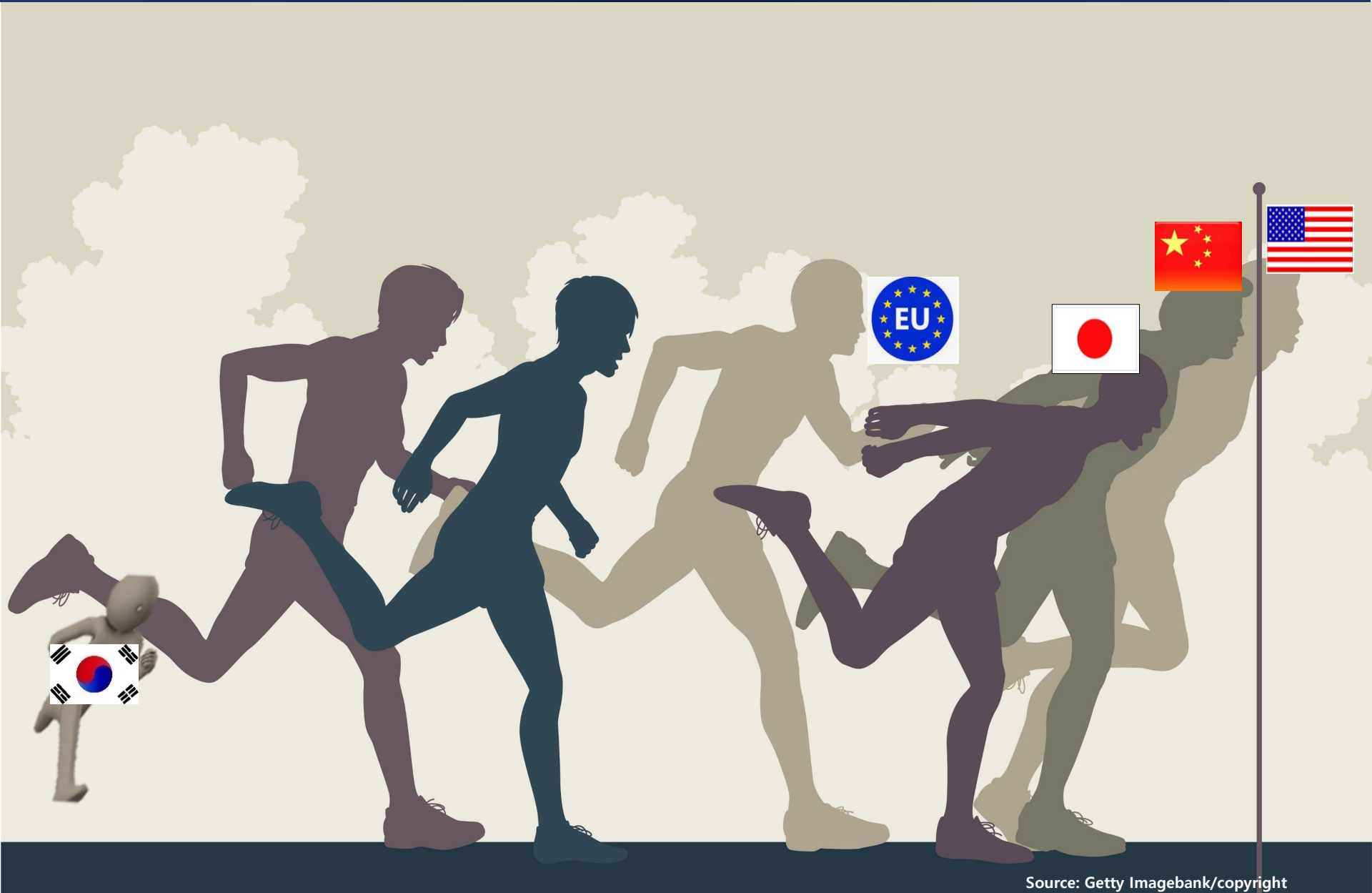
Advanced SoC
technology

Broader R&D eco-system

Post Supreme-K
Leap Forward ('25~'30)

*Exa-scale Supercomputing
Technology*

Reality: Where we are Now?



Thank you!
See you @SC24!

Key Technologies beyond exascale

