

Recent Advances in Open Fabric Interfaces

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OFI Insulates applications OFI – State of the Union from wide diversity of fabrics underneath PMDK[#], Spark[#], ZeroMQ[#], TensorFlow[#], Intel[®] MPI Sandia Clang Open MPI Chapel MPICH GASNet Charm++ MxNET[#], NetIO, Intel MLSL, rsockets ... SHMEM UPC SHMEM Library libfabric Enabled Middleware OFI Advanced application oriented semantics Scalable Multi-Shared Remote Unexpected Triggered Tag Matching Completion Address Message memory Receive Operations Buffering registration **Semantics** buffers Vectors **Reliable Datagram Endpoints** Streaming Endpoints RxM, RxD, **IBM Blue** AWS Network Shared Crav Sockets Cisco Intel Multi-Rail. Verbs Gen-Z* GNI* FFA* Gene* TCP, UDP usNIC OPA Memory Direct Hooks ...

Exploration

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Endpoint Accelerators Smart NICs, FPGA, GPU

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Expose common software APIs to apply data operations on network flows

Support offloaded accelerations in conjunction with network

- Smart NIC, FPGA, GPU, enhanced switches
- Local and/or remote accelerations
- Inline and look-aside

Discover available network functions

Enable functions at specific points in network data flows

This is not a general API for launching GPU/FPGA Kernels



Acceleration API requirements



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Proposal (WIP)

Introduce new provider capability

Extend attributes to request/report available accelerations

Introduce new OFI object that corresponds to an acceleration

- Network function
- Generic base definition

Specify network function with data transfers

- Apply to all transfers of a specific type
- Specify per operation



Network Functions



#define FI NETWORK FUNC (1ULL << ?)</pre>

```
struct fi_nf_info {
    struct fi_nf_info *next;
    int type;
    uint64_t caps;
    uint64_t flags;
    void *data;
    size_t data_len;
};
```

```
int fi_network_func(domain,
    struct fi_nf_info *nf_info,
    void * context,
    uint64_t flags,
    struct fid_nf **nf);
```

```
fi_ep_bind(ep, nf, flags);
e.g. flags = FI_SEND | FI_RECV
e.g. flags = FI_WRITE |
FI_REMOTE_WRITE
e.g. flags = 0
```

Open a network function

Associate the function with an endpoint Specify types of data transfers the function applies to

Or indicate that the function will be specified when submitting the transfer (flags=0)

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Network Functions

Specify function to apply to the current data transfer via existing context parameters Provide any needed input/output parameters



Re-use deferred work queues to execute long-running functions separate from data transfer

Assumes results will be used by future transfers

struct fi_deferred_work { ... }
fi_control(...)
FI_QUEUE_WORK
FI_SUBMIT_WORK
FI_CANCEL_WORK
FI_FLUSH_WORK

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Network Accelerators Collective Offloads, etc.



Motivation

Support *fabric* based offloads

Versus NIC based offloads

Immediate goal: accelerate collective operations

- SmartNIC / FPGA proposal focuses on endpoint accelerations
- This proposal focuses on network accelerations
- Separation is purely for convenience of discussion and focus

Solution should not be limited to collectives

Avoid trying to turn OFI into MPI



Network Accelerators



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Collective Groups



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Group Membership and Query



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Collective Operations

Initial set of collectives defined that can be accelerated

- Barrier: no data transferred
- Broadcast: flags indicate FI_SEND/RECV based on whether the process is root
- Allreduce: non-void datatype required
- We will look at defining order of reductions

ssize_t fi_broadcast(struct fid_ep *ep, void *buf, size_t count, void *desc, fi_addr_t coll_addr, enum fi_datatype dtype, enum fi_op op, uint64_t flags, void *context);

```
ssize_t fi_allreduce(..);
```

```
ssize_t fi_reduce_scatter(..);
```

```
ssize_t fi_alltoall(..);
```

```
ssize_t fi_allgather(..);
```

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Communication from Accelerators

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Overview

Support data transfers to/from/between peer devices

- GPUs, FPGAs, persistent memory
 - Examples only, solution is *mostly* independent from type of device
- PCI peer to peer transfers
 - E.g. GPU to RDMA NIC, GPU to GPU
 - Implementation agnostic, e.g. bounce buffers

Application examples:

Machine learning, deep learning, AI, MPI

Scope is limited to fabric communication (not trying to be the accelerator interface itself)



Related

Support libfabric running on non-host cores

Invoke accelerator functionality as part of transfer

Covered by separate SmartNIC proposal

File system backed memory regions

Transfers to/from storage without mapping file into process VA space



Definitions

Heterogeneous memory (HMEM)

- Non-host memory (e.g. PCI device memory)
- Unified address space



- Memory may be mapped into virtual address space of process
 - Without unified virtual address space, RMA may require FI_MR_RAW

Peer software interface

- Software interface to access peer device / allocate memory
- E.g. CUDA, OpenCL
- Compile and/or run time option?
- May need to support multiple SW interfaces simultaneously from single app





Requirements

SW may directly access HMEM device

- E.g. execute GPU kernels
- Most efficient if SW marks addresses as HMEM or not
 - Need to include device identifier

Middleware may lose HMEM association

- Rediscover HMEM properties
- Pass properties between app and OFI external from middleware
 - e.g. per-thread global variables

Memory *may* be allocated using specialized functions

e.g. cudaMalloc vs malloc





HMEM Hooking provider



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- OFI community is moving to intercept fabric offloads and compute accelerators
- The APIs being defined are generic and can be used for multiple vendors
- Collective Offload APIs offer both endpoint and switch accelerations
- Compute Accelerator APIs are in progress of being defined and will aim for both callable on Host and Accelerator cores
- Participation is OFIWG is free, simple and no boards to join

